

**HOT-555A Version 3.2**  
**Pentium™ processor**  
**Based PCI MAIN BOARD**  
*User's Manual*

## FCC Notice:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy. If not installed and used properly, in strict accordance with the manufacturer's instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures :

Reorient or relocate the receiving antenna.

Increase the separation between the equipment and receiver.

Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

Consult the dealer or an experienced radio/television technician for help and for additional suggestions.

The user may find the following booklet prepared by the Federal Communications Commission helpful "How to Identify and Resolve Radio-TV Interference Problems." This booklet is available from the U.S. Government Printing Office, Washington, DC 20402, Stock 004-000-00345-4

## FCC Warning

The user is cautioned that changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

*Note : In order for an installation of this product to maintain compliance with the limits for a Class B device, shielded cables and power cord must be used.*

## CE Notice:

Following standards were applied to this product, in order to achieve compliance with the electromagnetic compatibility :

- Immunity in accordance with EN 50082-1: 1992
- Emmissions in accordance with EN 55022: 1987 Class B.

## NOTICE

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*Manual Ver 2.0*

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# Preface

HOT-555A mainboard is a highly integrated IBM PC/AT compatible system board. The design will accept Intel Pentium, Intel Pentium MMX, Cyrix/IBM 6x86, 6x86L, 6x86MX and AMD K5/K6 processors and also features high-performance pipeline burst secondary cache memory support with size of 256KB and 512KB. The memory subsystem is designed to support up to 128 MB of EDO RAM, Standard Fast Page DRAM and SDRAM in standard 72-pin SIMM socket and 168-pin 3.3 V DIMM socket.

HOT-555A provides a new level of I/O integration. Intel's 82430VX PCIset chipset provides increased integration and improved performance over other chipset designs. The 82430VX PCIset chipset provides an integrated Bus Mastering IDE controller with two high performance IDE interfaces for up to four IDE devices.

The onboard Ultra I/O controller provides the standard PC I/O functions: Keyboard controller, R.T.C., floppy interface, two FIFO serial ports, an IrDA device port and a SPP/EPP/ECP capable parallel port.

Up to four PCI local bus slots provide a high bandwidth data path for data-movement intensive functions such as graphics, and up to three ISA slots complete the I/O function.

The HOT-555A provides the foundation for cost effective, high performance, highly expandable platforms, which deliver the latest in Pentium processor and I/O standard.

# Chapter 1 Introduction

## Specification

### CPU Function

- ☐ Pentium processors : 75~200MHz
- ☐ Pentium MMX processors : 150~233MHz
- ☐ Cyrix/IBM 6x86 processors : PR120~PR166
- ☐ Cyrix/IBM 6x86L processors : PR120~PR166
- ☐ Cyrix/IBM 6x86MX processors : PR166~PR266
- ☐ AMD-K5 processors : PR75~PR200
- ☐ AMD-K6 processors : 166~266MHz

### Chipset

- ☐ Intel PCIsset 82437VX, 82438VX and 82371SB

### Memory

- ☐ Provides four 72-pin SIMM sockets for 5V EDO and Fast Page Mode SIMMs  
Supports 4MB, 8MB, 16MB, 32MB 72-pin SIMMs ranging from 8MB to 128MB
- ☐ Provides two 168-pin DIMM sockets for 3.3V Sync. DRAM, EDO or Fast Page Mode DIMMs  
Supports 8MB, 16MB, 32MB and more 168-pin DIMMs

### Cache Memory

- ☐ Integrated L2 write-back cache controller
  - 512KB or 256KB(option) Direct Mapped Pipeline Burst Cache

### Onboard Regulator

- ☐ High efficiency switching mode regulator provides steady 3V ranging voltage and 10 Amp current

## Power Management Function

- ☐ Provides three stages power management mode : Doze, Standby, and Suspend
- ☐ Supports Microsoft APM Ver 1.2
- ☐ Provides EPMI (External Power Management Interrupt) pin

## Expansions

- ☐ 32-bit PCI bus slot x 4
- ☐ 16-bit ISA bus slot x 3
- ☐ 2-channel PCI IDE port
  - Support up to 4 IDE devices
  - PIO Mode 4, DMA Mode 2 transfers up to 22 MB/sec
  - Integrated 8 x 32-bit buffer for PCI IDE burst transfers
- ☐ One floppy port
- ☐ One parallel port
  - Supports **SPP** (PS/2 compatible bidirectional Parallel Port), **EPP** (Enhanced Parallel Port), and **ECP** (Extended Capabilities Port) high performance parallel port.
- ☐ Two serial ports
  - Supports 16C550 compatible UARTS.
  - Supports IrDA (Infra-red) communication.
- ☐ One PS/2 mouse port
- ☐ Two USB (Universal Serial Bus) ports

## System BIOS

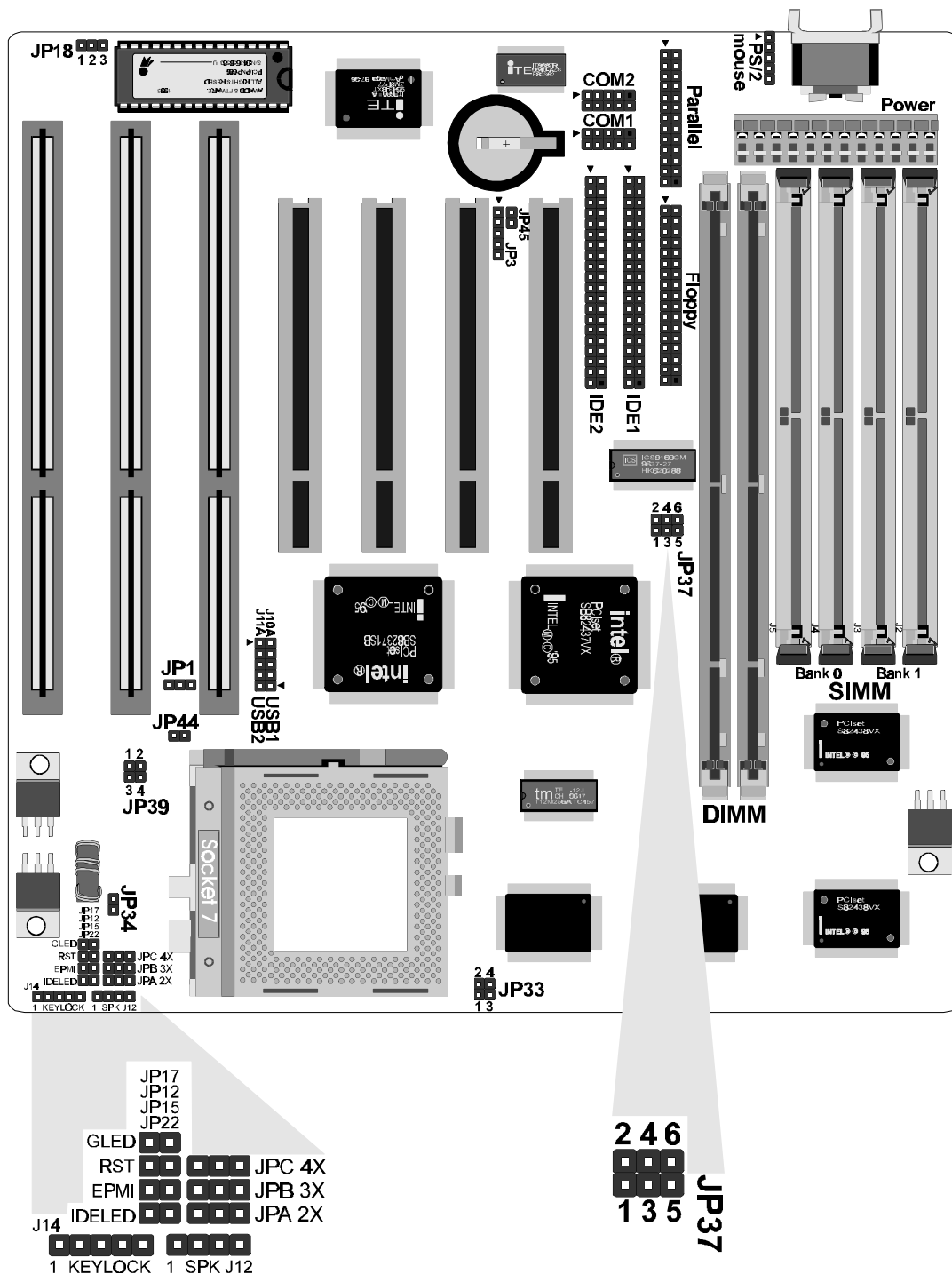
- ☐ Award PnP BIOS v4.51PG  
Bundled with Symbios Login(NCR) SDCM V4.0 SCSI BIOS

## Board Design





- ☐ Dimension 220mm x 230mm



# Chapter 2 Hardware Configuration

## HOT-555A Version 3.2 Layout



## Jumpers

Several hardware settings are made through the use of jumper caps to connect jumper pins on the main board. The jumper's pin 1 on main board will be on the top or on the left when holding the main board with the keyboard connector away from yourself. Pinout numeric is written around the jumpers with four or six pin jumpers. The jumpers will be show graphically such as  to connect pins 3&4 and 5&6, and  to connect pins 1&2 and 3&4 for six pin jumpers. Jumpers will be show graphically such as  to connect pins 2&4 and  to connect pins 3&4 for four pin jumpers.

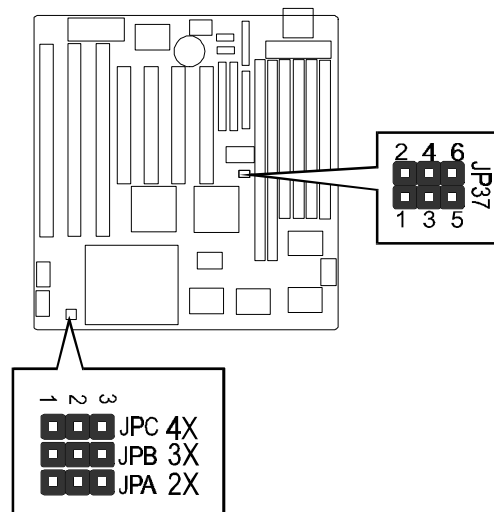
Jumpers with two pins will be shown as  for Short (On) and  for Open (Off).

To connect the pins, simply place a plastic jumper cap over the two pins as diagramed.

## CPU Clock Speed Selection - JP37, JPA, JPB and JPC

HOT-555A mainboard features a clock generator to provide adjustable system clock frequency. JP37 is a 6-pins jumper which determine the system clock frequency from 50 MHz to 66 MHz.

HOT-555A mainboard also provides Jumpers JPA(BF0), JPB(BF1) and JPC(BF2) to figure the CPU core clock multiplier. By inserting jumper caps on JPA, JPB and JPC, the user can change the **Host Bus Clock/CPU Core Clock** ratio from 1 : 1.5 to 1 : 4.





## CPU Clock Configuration

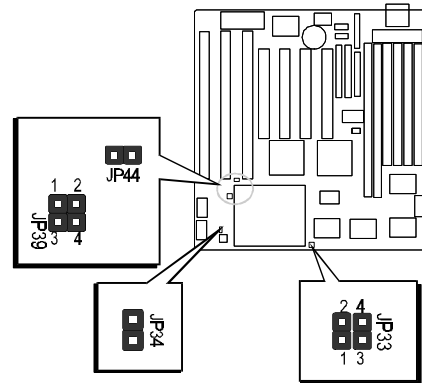
Processors	JP37	System Clock / Multiplier	Frequency Multiplier JPA, JPB, JPC
AMD-K6 266 MHz		66 MHz x 4	
Pentium MMX 233 MHz AMD-K6 233 MHz Cyrix/IBM 6x86MX-PR266		66 MHz x 3.5	
Pentium MMX 200 MHz Pentium 200 MHz AMD-K6 200 MHz AMD-K5 PR200 Cyrix/IBM 6x86MX-PR233		66 MHz x 3	
Pentium MMX 166 MHz Pentium 166 MHz AMD-K6 166 MHz AMD-K5 PR166 Cyrix/IBM 6x86MX-PR200		66 MHz x 2.5	
Pentium MMX 150 MHz Pentium 150 MHz AMD-K5 PR150 Cyrix/IBM 6x86MX-PR166		60 MHz x 2.5	
Pentium 133 MHz		66 MHz x 2	
Cyrix/IBM 6x86L P166+ Cyrix/IBM 6x86 P166+		66 MHz x 2	
Pentium 120 MHz		60 MHz x 2	
Cyrix/IBM 6x86L P150+ Cyrix/IBM 6x86 P150+		60 MHz x 2	
Cyrix/IBM 6x86 PR133		55 MHz x 2	
Cyrix/IBM 6x86 P120+		50 MHz x 2	
Pentium 100 MHz AMD-K5 PR133 AMD-K5 PR100		66 MHz x 1.5	
Pentium 90 MHz AMD-K5 PR120 AMD-K5 PR90		60 MHz x 1.5	
Pentium 75 MHz AMD-K5 PR75		50 MHz x 1.5	

## Onboard Regulator Output- JP39, JP34, JP33 and JP44

These jumpers set the voltage supplied to the processor. Intel Pentium STD has only a Single Power Plane and uses the standard 3.3V or Pentium VRE uses the 3.52V, AMD K5 and Cyrix/IBM 6x86 has also have a single power plane and use 3.52V.

Currently Intel's new Pentium P55C MMX, AMD K6 and Cyrix/IBM 6x86L with dual power planes, Pentium P55C MMX and Cyrix/IBM 6x86L requires 2.8V, AMD K6 166 and 200 require 2.9V; 233 requires 3.2V.

JP44 is designed to fine tune  $V_{CORE}$  output from regulator. When the jumper cap is removed from JP44, it will increase  $V_{CORE}$  voltage output from regulator by 2.5%. Normally, JP44 is set to close(ON) by insert a jumper cap.



### Dual Power Planes ( $V_{IO}$ , $V_{CORE}$ separated)

Processor	Vcore Output	JP39	JP33	JP34
Pentium MMX 150~233 MHz, Cyrix/IBM 6x86L PR150 / PR166 Cyrix/IBM 6x86MX PR166~PR266	2.8 V			
AMD-K6 166 / 200 MHz	2.9 V			
AMD-K6 233 / 266 MHz	3.2 V			

### Single Power Plane ( $V_{IO}=V_{CORE}$ )

Processor	Vcore Output	JP39	JP33	JP34
Pentium 75~200 MHz (STD), Cyrix/IBM 6x86 PR120~166 (3.3V)	3.3 V			
Pentium 75~200 MHz (VRE), Cyrix/IBM 6x86 PR120~166, AMD-K5 PR75~200	3.52 V			

## **Flash EPROM Vpp Jumper - JP18**

HOT-555A mainboard supports two types of flash EPROM: 5 volt and 12 volt. By setting up jumper JP18, you can update both types of flash EPROM with new system BIOS files as they come available.  
JP18 Pin 2-3 Close for 5V, Pin 1-2 Close for 12V.

## **BIOS UPGRADES**

Flash memory makes distributing BIOS upgrades easy. A new version of BIOS can be installed from a diskette.

Please note the following when making the BIOS updates.

- \*\* Flash utility must work under real mode. Memory manager like **QEMM.386**, **EMM386** should not be loaded. (or Simply bypass all **config.sys** and **autoexec.bat** on system boot up)
- \*\* Flash utility supports both 5V and 12V Flash EEPROM.

## **Clear CMOS - JP45**

This jumper can clear the CMOS data stored in the Ultra I/O chip. To clear the CMOS data please follow listed steps:

- 1) Turn off the PC,
- 2) Remove the jumper cap from JP45 for a brief while,
- 3) Reinsert the jumper cap to JP45,
- 4) Turn on the PC.

## **Connectors & Sockets**

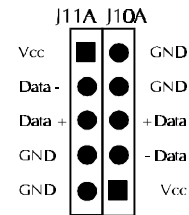
**Connectors & Sockets**

ITEM	FUNCTION	ITEM	FUNCTION
SIM 1, 2, 3, 4	On-board SIMM sockets	J14	Power LED and Keylock Connector
DIM 1, 2	On-board 3.3V DIMM sockets	J12	PC Speaker Connector
J17,18,19,20	On-board PCI Slots	JP12	Hardware Reset Switch Connector
J21, 22, 23	On-board ISA Slots	JP33	Green LED
J6	On-board PCI Primary IDE Connector	JP15	EPMI Connector
J7	On-board PCI Secondary IDE Connector	JP22	On-board Enhanced IDE R/W LED Connector
CN1	On-board Floppy Controller Connector	J10A, J11A	Universal Serial Bus (USB) Connectors *Note 1
CN4	On-board Parallel Port Connector	JP3	Infra-red Communication Port Connector *Note 2
CN2	On-board Serial port-1 Connector	JP1	Cooling Fan Connector *Note 3
CN3	On-board Serial Port-2 Connector	J99	On-board PS/2 Mouse Port Connector *Note 4

**Note 1: J10A, J11A - USB connectors**

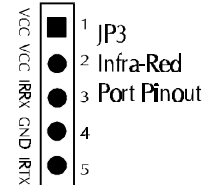
The main board provides two sets USB (Universal Serial Bus) connectors - J10A and J11A for USB devices use.

**USB Connectors Pin-out**



**Note 2: JP3 - Infrared module connector**

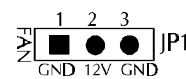
The main board provides a 5-pin infrared connector - JP3 as an optional infrared module for wireless transmitting and receiving.



**Note 3: JP1 - 12V cooling fan power connector**

The main board provides a on-board 12V cooling fan power connector for cooling fan. Please make sure the red wire connect to +12V and black wire connect to ground (GND).

**Onboard Cooling Fan Connector Pin-out**

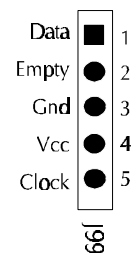


**Caution : Do not short 12V and GND pin of JP1 by a jumper cap** or it will cause serve damage to the main board.

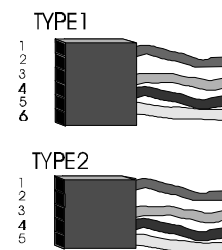
**Note 4: JP99- PS/2 Mouse 5 pins connector**

The main board provides an 5 pins PS/2 mouse connector for optional PS/2 mouse cable. Diagram on the right side indicates the pinout of the connector.

HOT-555A mainboard supplies two types of optional PS/2 mouse adapter cable, type 1 with 6-holes plug which hole 2 and hole 6 are wireless; type 2 with 5-holes plug which hole 2 is wireless.



**Caution :** When a PS/2 mouse is used, make sure connect PS/2 mouse adapter cable hole 1 to the pin 1 of onboard PS/2 connector (J99). Reversed connecting may cause damage to your PS/2 mouse.



## Chapter 3 Memory Configuration

The HOT-555A mainboard provides four 72-pin SIMM sockets and two 168-pin DIMM sockets that make it possible to install up to 128MB of RAM. The SIMM socket support 4MB, 8MB, 16MB, and 32MB 5V single- or double-side Fast Page or EDO DRAM modules, and DIMM socket support 8MB, 16MB, 32MB, . . ., 3.3V single- or double-side SDRAM, Fast Page, or EDO modules.

***Caution : The user should not populate both 5V SIMM modules & 3.3V DIMM modules at the same time.***

The four SIMM sockets are arranged in two banks of two sockets each, the two DIMM sockets are also arranged in two banks of each socket. Each bank provides a 64/72-bit wide data path.

Both SIMMs in a bank must be of the same memory size and type, although the different types of memory may differ between banks. It is possible to have 70 ns fast page DRAM in one bank and 60 ns EDO DRAM in the other.

The memory configuration tables on next two pages list the SIMMs and DIMMs memory configuration.

**Table 3-1. Memory Configuration Table For SIMMs**

<b>SIM 1</b>	<b>SIM 2</b>	<b>SIM 3</b>	<b>SIM 4</b>	<b>TOTAL</b>
4 MB	4 MB	——	——	8 MB
——	——	4 MB	4 MB	8 MB
4 MB	4 MB	4 MB	4 MB	16 MB
8 MB	8 MB	——	——	16 MB
——	——	8 MB	8 MB	16 MB
4 MB	4 MB	8 MB	8 MB	24 MB
8 MB	8 MB	4 MB	4 MB	24 MB
8 MB	8 MB	8 MB	8 MB	32 MB
16 MB	16 MB	——	——	32 MB
——	——	16 MB	16 MB	32 MB
4 MB	4 MB	16 MB	16 MB	40 MB
16 MB	16 MB	4 MB	4 MB	40 MB
8 MB	8 MB	16 MB	16 MB	48 MB
16 MB	16 MB	8 MB	8 MB	48 MB
16 MB	16 MB	16 MB	16 MB	64 MB
32 MB	32 MB	——	——	64 MB
——	——	32 MB	32 MB	64 MB
4 MB	4 MB	32 MB	32 MB	72 MB
32 MB	32 MB	4 MB	4 MB	72 MB
8 MB	8 MB	32 MB	32 MB	80 MB
32 MB	32 MB	8 MB	8 MB	80 MB
16 MB	16 MB	32 MB	32 MB	96 MB
32 MB	32 MB	16 MB	16 MB	96 MB
32 MB	32 MB	32 MB	32 MB	128 MB

**Table 3-2 Memory Configuration Table For DIMMs**

<b>DIM 1</b>	<b>DIM 2</b>	<b>TOTAL</b>
8 MB	——	8 MB
——	8 MB	8 MB
16 MB	——	16 MB
——	16 MB	16 MB
8 MB	16 MB	24 MB
16 MB	8 MB	24 MB
32 MB	——	32 MB
——	32 MB	32 MB
8 MB	32 MB	40 MB
32 MB	8 MB	40 MB
16 MB	32 MB	48 MB
32 MB	16 MB	48 MB
32 MB	32 MB	64 MB
...	...	...
...	...	...
...	...	...
...	...	...

## Chapter 4 Award BIOS Setup

HOT-555A BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed RAM so that it retains the Setup information when the power is turned off.

### Entering Setup

Power on the computer and press <Del> immediately will allow you to enter Setup. The other way to enter Setup is to power on the computer, when the below message appear briefly at the bottom of the screen during the POST (Power On Self Test), press <Del> key or simultaneously press <Ctrl>,<Alt>, and <Esc> keys.

#### **TO ENTER SETUP BEFORE BOOT PRESS CTRL-ALT-ESC OR DEL KEY**

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF the ON or pressing the "RESET" button on the system case. You may also restart by simultaneously press <Ctrl>,<Alt>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message will be displayed and you will again be asked to,

#### **PRESS F1 TO CONTINUE, CTRL-ALT-ESC OR DEL TO ENTER SETUP**



## **The Main Menu**

ROM PCI/ISA BIOS (2A59GH2K) CMOS SETUP UTILITY AWARD SOFTWARE, INC.	
STANDARD CMOS SETUP	INTEGRATED PERIPHERALS
BIOS FEATURES SETUP	IDE HDD AUTO DETECTION
CHIPSET FEATURES SETUP	SUPERVISOR PASSWORD
POWER MANAGEMENT SETUP	USER PASSWORD
PNP/PCI CONFIGURATION	SAVE & EXIT SETUP
LOAD BIOS DEFAULTS	EXIT WITHOUT SAVING
LOAD SETUP DEFAULTS	
Esc : Quit	↑ ↓ → ← : Select Item
F10 : Save & Exit Setup	(Shift)F2 : Change Color

### **Standard CMOS setup**

This setup page includes all items in a standard compatible BIOS.

### **BIOS features setup**

This setup page includes all items of Award special enhanced features.

### **Chipset features setup**

This setup page includes all items of chipset features.

### **Power Management Setup**

This setup page includes all items of Power Management features.

### **PCI Configuration setup**

This item specifies the value (in units of PCI bus blocks) of the latency timer for the PCI bus master and the IRQ level for PCI device. Power-on with BIOS defaults

### **Load BIOS Defaults**

BIOS defaults loads the values required by the system for the maximum performance. However, you may change the parameter through each Setup Menu.

### **Load Setup Defaults**

Setup defaults loads the values required by the system for the O.K. performance. However, you can change the parameter through each Setup Menu.

### **Integrated Peripherals**

This setup page includes all items of peripheral features.

### **IDE HDD auto detection**

Automatically configure IDE hard disk drive parameters.

### **Supervisor Password**

Change, set, or disable supervisor password. It allows you to limit access to the system and Setup, or just to Setup.

### **User Password**

Change, set, or disable user password. It allows you to limit access to the system and Setup, or just to Setup.

### **Save & Exit setup**

Save CMOS value change to CMOS and exit setup

### **Exit without saving**

Abandon all CMOS value changes and exit setup.

## Standard CMOS Setup

ROM PCI/ISA BIOS (2A59GH2K)									
STANDARD CMOS SETUP									
AWARD SOFTWARE, INC.									
Date (mm:dd:yy) : Mon, Jan 20 1997									
Time (hh:mm:ss) : 15 : 7 : 2									
HARD DISKS	TYPE	SIZE	CYLS	HEAD	PRECOMP	LANDZ	SECTOR	MODE	
Primary Master	: Auto	0	0	0	0	0	0	0	AUTO
Primary Slave	: Auto	0	0	0	0	0	0	0	AUTO
Secondary Master	: Auto	0	0	0	0	0	0	0	AUTO
Secondary Slave	: Auto	0	0	0	0	0	0	0	AUTO
Drive A : 1.44M, 3.5 in.									
Drive B : None									
Video : EGA/VGA									
Halt On : All Errors									
			Base Memory:				0K		
			Extended Memory:				0K		
			Other Memory:				512K		
			Total Memory:				512K		
ESC : Quit		↑ ↓ → ← : Select Item			PU/PD/+/- : Modify				
F1 : Help		(Shift)F2 : Change Color							

### Date

The date format is <day>, <month> <date> <year>. Press <F3> to show the calendar.

### Time

The time format is <hour> <minute> <second>. The time is calculated base on the 24-hour military-time clock. For example. 5 p.m. is 17:00:00.

### Drive C type/Drive D type

This item identify the types of hard disk drive C and drive D that has been installed in the computer. There are 46 predefined types and a user definable type.

Press PgUp or PgDn to select a numbered hard disk type or type the number and press <Enter>. Note that the specifications of your drive must match with the drive table. The hard disk will not work properly if you enter improper information for this item. If your hard disk drive type is not matched or listed, you can manually use Type User to define your own drive type.

If you select Type User, related information is asked to be entered to the following items. Enter the information directly from the keyboard and press <Enter>. This information should be provided in the documentation from your hard disk vendor or the system manufacturer.

The user may also set those items to AUTO to auto configure hard disk drives parameter when system power-on.

If a hard disk drive has not been installed select NONE and press <Enter>.

### **Drive A type/Drive B type**

This item specifies the types of floppy disk drive A or drive B that has been installed in the system.

### **Video**

This item selects the type of adapter used for the primary system monitor that must matches your video display card and monitor. Although secondary monitors are supported, you do not have to select the type in Setup.

### **Error halt**

This item determines if the system will stop, when an error is detected during power up.

### **Memory**

This item is display-only. It is automatically detected by POST (Power On Self Test) of the BIOS.

#### **Base Memory**

The POST of the BIOS will determine the amount of base (or conventional) memory installed in the system. The value of the base memory is typically 512K for systems with 512K memory installed on the mainboard, or 640K for systems with 640K or more memory installed on the mainboard.

#### **Extended Memory**

The BIOS determines how much extended memory is present during the POST. This is the amount of memory located above 1MB in the CPU's memory address map.

## **BIOS Features Setup**

ROM PCI/ISA BIOS (2A59GH2K) BIOS FEATURES SETUP AWARD SOFTWARE, INC.			
CPU Internal Cache	: Enabled	Video BIOS Shadow	: Enabled
External Cache	: Enabled	C8000-CBFFF Shadow	: Disabled
Quick Power On Self Test	: Enabled	CC000-CFFFF Shadow	: Disabled
Boot Sequence	: A,C,SCSI	D0000-D3FFF Shadow	: Disabled
Swap Floppy Drive	: Disabled	D4000-D7FFF Shadow	: Disabled
Boot Up Floppy Seek	: Enabled	D8000-DBFFF Shadow	: Disabled
Boot Up NumLock Status	: On	DC000-DFFFF Shadow	: Disabled
Boot Up System Speed	: High		
Gate A20 Option	: Fast		
TypeMatic Rate Setting	: Disabled		
TypeMatic Rate (Chars/Sec)	: 6		
TypeMatic Delay (Msec)	: 250		
Security Option	: Setup		
PS/2 mouse function control	: Disabled		
PCI/UGA Palette Snoop	: Disabled		
OS Select For DRAM > 64MB	: Non-OS2		
		ESC : Quit	↑↓→← : Select Item
		F1 : Help	PU/PD/+/- : Modify
		F5 : Old Values	(Shift)F2 : Color
		F6 : Load BIOS Defaults	
		F7 : Load Setup Defaults	

### **CPU Internal/External Cache**

This item enables CPU internal/External cache to speed up memory access.

### **Quick Power On Self Test**

This item speeds up Power On Self Test (POST) after you power on the computer. If it is set to Enabled, BIOS will shorten or skip some check items during POST.

### **Boot Sequence**

This item determines which drive computer searches first for the disk operating system. Default value is A, C, SCSI.

### **Swap Floppy Drive**

When this item enables, the BIOS will swap floppy drive assignments so that Drive A: will function as Drive B: and Drive B: as Drive A:.

### **Boot Up Floppy Seek**

During POST, BIOS will determine if the floppy disk drive installed is 40 or 80 tracks.

### **Boot Up NumLock Status**

When this option enables, BIOS turns on *Num Lock* when system is powered on.

### **Boot Up System Speed**

This option sets the speed of the CPU at system boot time. The settings are *High* or *Low*.

### **Gate A20 Option**

When this item sets on Normal, the A20 signal is controlled by keyboard controller. When this item sets on Fast, the A20 signal is controlled by post 92 or chipset specific method.

### **Typematic Rate Setting/Typematic Rate/Typematic Delay**

This determines if the typematic rate and typematic delay are to be used. When the typematic rate setting is enabled, **typematic rate** allows you select the rate at which the keys are accelerated and **typematic delay** allows you to select the delay between when the key was first depressed and when the acceleration begins.

### **Security Option**

This item allows you to limit access to the System and Setup, or just to Setup. When **System** is selected, the System will not boot and access to Setup will be denied if the correct password is not entered at the prompt. When **Setup** is selected, the System will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

### **PS/2 Mouse Control Function**

Use this item to set the PS/2 mouse. If there is a PS/2 mouse attached to your system, this item must be enabled, if not, please disabled this item to release IRQ12 for PCI device.

### **PCI VGA Palette Snoop**

This item must be set to enabled if there is a MPEG ISA card installed in the system, and disabled if there is no MPEG ISA card installed in the system.

### **OS Select For DRAM > 64MB**

This item allows you to access the memory that over 64 MB in OS/2.

### **Video BIOS Shadow/XXXXX-XXXXX Shadow**

These items determine whether Video BIOS or optional ROM will be copied to RAM.

## Chipset Features Setup

ROM PCI/ISA BIOS (2A59GH2K) CHIPSET FEATURES SETUP AWARD SOFTWARE, INC.			
Auto Configuration	: Enabled	Delayed Transaction	: Disabled
DRAM Timing	: 70ns		
DRAM RAS# Precharge Time	: 4		
DRAM R/W Leadoff Timing	: 6		
Fast RAS To CAS Delay	: 3		
DRAM Read Burst (EDO/FP)	: x222/x333		
DRAM Write Burst Timing	: x333		
Fast MA to RAS# Delay CLK	: 1		
Fast EDO Path Select	: Disabled		
Refresh RAS# Assertion	: 5 Clks		
ISA Bus Clock	: PCICLK/4		
SDRAM(CAS Lat/RAS-to-CAS)	: 3/3		
System BIOS Cacheable	: Disabled		
Video BIOS Cacheable	: Disabled		
8 Bit I/O Recovery Time	: 3	ESC : Quit	↑↓←→ : Select Item
16 Bit I/O Recovery Time	: 2	F1 : Help	PU/PD/+/- : Modify
Memory Hole At 15M-16M	: Disabled	F5 : Old Values	(Shift)F2 : Color
Peer Concurrency	: Enabled	F6 : Load BIOS Defaults	
Passive Release	: Enabled	F7 : Load Setup Defaults	

### Auto Configuration

This item auto configures the following items: DRAM RAS# Precharge time, DRAM R/W Leadoff Timing, Fast RAS to CAS Delay, DRAM Read Burst, DRAM Write Burst Timing, Fast MA to RAS# Delay CLK, Fast EDO Path Select, Refresh RAS# Assertion, and ISA Bus Clock by different system clock.

### DRAM Timing

This item set the DRAM Read/Write timings that the system uses. When item, "Auto Configuration", is disabled, this item will not show up.

### DRAM RAS# Precharge Time

DRAM must continually be refreshed or it will lose its data. Normally, DRAM is refreshed entirely by a single request. This option allows you to determine the number of CPU clocks allocated for Row Address Strobe to accumulate its charge before the DRAM is refreshed. If insufficient time is allowed, refresh may be incomplete and data lost.

This item sets the DRAM RAS Precharge Timing. The options are **4** and **3** CLKs.

### DRAM R/W Leadoff Timing

This item sets the number of CPU clocks allowed before DRAM Reads and Writes are performed.

### **Fast RAS To CAS Delay**

When DRAM is refreshed, both rows and columns are address separately. This setup item allows you to determine the timing of the transition from Row Address Strobe (RAS) to Column Address Strobe (CAS). The options are **3** and **2** CLKs.

### **DRAM Read Burst (EDO/FP)**

This item set the EDO/FP DRAM Read Burst Timing. The timing used depends on the type of DRAM (EDO burst mode or standard fast page mode) on a per-bank basis. The options are **x222/x333**, **x333/x444**, and **x444/x444**.

### **DRAM Write Burst Timing**

This item set the DRAM Write Burst Timing. The timing used depends on the type of DRAM (standard page mode or EDO burst mode) on a per-bank basis. The options are **x4444**, **x3333**, and **x2222**.

### **Fast MA to RAS# Delay CLK**

This item is used to set Fast MA (Memory Address) to RAS# Delay which control DRAM Row Miss timings.

### **Fast EDO Path Select**

This item is used to defined which fast path is selected for CPU to DRAM read cycles for leadoff, the options are "**Enable**" or "**Disable**".

### **Refresh RAS# Assertion**

This item is used to set the number of clocks RAS# is asserted for Refresh cycles.

### **SDRAM (CAS Lat/RAS-to-CAS)**

This item is used to set CAS# Latency and RAS# to CAS# clock for SDRAM. If SDRAMs absent, this item will not show up.

### **ISA Clock**

This item allows the user to set ISA clock that divide from PCI clock by 3 or by 4. For example, if 166MHz Pentium processor is used, PCI clock will be 33MHz, ISA Clock will be 8.25MHz when PCI clock is divided by 4, and 11MHz when PCI clock is divided by 3.



### **System BIOS Cacheable**

This item allows the user to set the system BIOS F000~FFFF areas that are cacheable or non-cacheable.

### **Video BIOS Cacheable**

This item allows the user to set the video BIOS C000~C7FF areas that are cacheable or non-cacheable.

### **8 Bit I/O Recovery Time**

The recovery time is the length of time, measured in CPU clocks, that the system will delay after the completion of an input/output request. This delay takes place because the CPU is operating more than the input/output bus that the CPU must be delayed to allow for the completion of the I/O.

This item allows you to determine the recovery time allowed for 8 bit I/O. Choices are from NA, 1 to 8 CPU clocks.

### **16-Bit I/O Recovery Time**

This item allows you to determine the recovery time allowed for 16 bit I/O. Choices are from NA, 1 to 4 CPU clocks.

### **Memory Hole At 15M-16M**

In order to improve performance, some space in memory can be reserved for ISA cards. This memory must be mapped into the memory space below 16 MB.

### **Peer Concurrency**

Peer concurrency means that more than one PCI device can be active at a time. Enabling this item allows multiple PCI devices to be active.

### **Passive Release**

When enabled, the chipset provides a programmable passive release mechanism to meet the required ISA master latencies.

### **Delayed Transaction**

Since the 2.1 revision of the PCI specification requires much tighter controls on target and master latency. PCI cycles to or from ISA typically take longer. When enabled, the chipset provides a programmable delayed completion mechanism to meet the required target latencies.

## Power Management Setup

ROM PCI/ISA BIOS (2A59GH2K)	
POWER MANAGEMENT SETUP	
AWARD SOFTWARE, INC.	
Power Management	: Disable
PM Control by APM	: Yes
Video Off Method	: V/H SYNC+Blank
MODEM Use IRQ	: 3
Doze Mode	: Disable
Standby Mode	: Disable
Suspend Mode	: Disable
HDD Power Down	: Disable
** Wake Up Events In Doze & Standby **	
IRQ3 (Wake-Up Event)	: ON
IRQ4 (Wake-Up Event)	: ON
IRQ8 (Wake-Up Event)	: ON
IRQ12 (Wake-Up Event)	: ON
** Power Down & Resume Events **	
IRQ3 (COM 2)	: ON
IRQ4 (COM 1)	: ON
IRQ5 (LPT 2)	: OFF
IRQ6 (Floppy Disk)	: OFF
IRQ7 (LPT 1)	: OFF
IRQ8 (RTC Alarm)	: OFF
IRQ9 (IRQ2 Redir)	: OFF
IRQ10 (Reserved)	: OFF
IRQ11 (Reserved)	: OFF
IRQ12 (PS/2 Mouse)	: OFF
IRQ13 (Coprocessor)	: OFF
IRQ14 (Hard Disk)	: ON
IRQ15 (Reserved)	: OFF
ESC : Quit            ↑↓→← : Select Item	
F1 : Help            PU/PD/+/- : Modify	
F5 : Old Values    (Shift)F2 : Color	
F6 : Load BIOS Defaults	
F7 : Load Setup Defaults	

### Power Management

This item determines the options of the power management function. Default value is Disable. The following pages tell you the options of each item and describe the meanings of each options.

**Disabled** Global Power Management will be disabled.

**User Define** Users can configure their own power management.

**Min Saving** Predefined timer values are used such that all timers are in their maximum value.

**Max Saving** Predefined timer values are used such that all timers minimum value.

### PM Control by APM

If this item set to No, system BIOS will be ignored and APM calls the power to manage the system. If this item is setup to Yes, system BIOS will wait for APM's prompt before it enter any PM mode e.g. **DOZE**, **STANDBY** or **SUSPEND**.

### Video Off Method

**Blank Screen** The system BIOS will only blanks off the screen when disabling video.

**V/H SYN +Blank** In addition to Blank Screen, BIOS will also turn off the V-SYNC & H-SYNC signals from VGA cards to monitor.

**DPMS** This function is enabled for only the VGA card supporting DPM.

### **Doze Mode**

- 1 Min~1 Hr** Defines the continuous idle time before the system enters DOZE mode.
- Disable** System will never enter DOZE mode.

### **Standby Mode**

- 1 Min~1 Hr** Defines the continues idle time before the system enters STANDBY mode.
- Disable** System will never enter STANDBY mode.

### **Suspend Mode**

- 1 Min~1 Hr** Defines the continuous idle time before the system enters SUSPEND mode.
- Disable** System will never enter SUSPEND mode.

### **HDD Power Down**

- 1~15Min** Defines the continuous HDD idle time before the HDD enters power saving mode (motor off).
- Disable** HDD's motor will not be turn off.

### **IRQ3, 5, 8, 12 \*\*Wake-Up Events In Doze & Standby\*\***

If these items set on Off, the IRQ3, 5, 8 or 12 event's activity will not reactivates the system from Doze and Standby mode.

If these items set on On, the IRQ3, 5, 8 or 12 event's activity will reactivate system from Doze and Standby mode.

### **\*Power Down & Resume Events \*\***

If this items is set to Off, the event's activity will not be monitored by entering power management.

If this items is set to On, the event's activity will be monitored by entering power management.

COM Post Accessed	LPT Ports Accessed	Drive Ports Accessed
IRQ 3 (COM 2)	IRQ 4 (COM1)	IRQ 5 (LPT 2)
IRQ 6 (Floppy Disk)	IRQ 7 (LPT 1)	IRQ 8 (RTC Alarm)
IRQ 9 (IRQ 2 Redir)	IRQ 10 (Reserved)	IRQ 11 (Reserved)
IRQ 12 (PS/2 Mouse)	IRQ 13(Copro-)	IRQ 14 (Hard Disk)
IRQ 15 (Reserved)		

## PCI Configuration Setup

ROM PCI/ISA BIOS (2A59GH2K) PNP/PCI CONFIGURATION AWARD SOFTWARE, INC.	
PNP OS Installed : <b>No</b>	PCI IRQ Activated By : Level
Resources Controlled By : Manual	PCI IDE IRQ Map To : PCI-AUTO
Reset Configuration Data : Disabled	Primary IDE INT# : A
	Secondary IDE INT# : B
IRQ-3 assigned to : Legacy ISA	
IRQ-4 assigned to : Legacy ISA	
IRQ-5 assigned to : PCI/ISA PnP	
IRQ-7 assigned to : PCI/ISA PnP	
IRQ-9 assigned to : PCI/ISA PnP	
IRQ-10 assigned to : PCI/ISA PnP	
IRQ-11 assigned to : PCI/ISA PnP	
IRQ-12 assigned to : PCI/ISA PnP	
IRQ-14 assigned to : PCI/ISA PnP	
IRQ-15 assigned to : PCI/ISA PnP	
DMA-0 assigned to : PCI/ISA PnP	
DMA-1 assigned to : PCI/ISA PnP	ESC : Quit      ↑↓+* : Select Item
DMA-3 assigned to : PCI/ISA PnP	F1 : Help      PU/PD/+/- : Modify
DMA-5 assigned to : PCI/ISA PnP	F5 : Old Values (Shift)F2 : Color
DMA-6 assigned to : PCI/ISA PnP	F6 : Load BIOS Defaults
DMA-7 assigned to : PCI/ISA PnP	F7 : Load Setup Defaults

### PNP OS Installed

When this item is set to **Yes**, it allows the PnP OS(Windows 95) control the System resources except PCI devices and PnP boot devices.  
Default setting is **No**.

### Resources Controlled By

The Award Plug and Play BIOS has the capability to automatically configure all of the boot and Plug and Play compatible devices.

### Reset Configuration Data

This item allows you to determine whether to reset the configuration data or not.

### IRQ 3/4/5/7/9/10/11/12/14/15, assigned to

These items allow you to determine the IRQ assigned to the ISA bus and is not available for PCI slot.  
Choices are **Legacy ISA** and **PCI/ISA PnP**.

### DMA 0/1/3/5/6/7 assigned to

These items allow you to determine the DMA assigned to the ISA bus and is not available for PCI slot.  
Choices are **Legacy ISA** and **PCI/ISA PnP**.

### **PCI IRQ Activated by**

This item sets the method by which the PCI bus recognize that an IRQ service is being requested by a device. you should never change the default configuration unless advised otherwise by your system's manufacturer. Choices are *Level*(default) and *Edge*.

### **PCI IDE IRQ Map to**

This items allows you to configure your system to the type of IDE disk controller in use. By default, Setup assumes that your controller is an ISA device rather than a PCI controller.

If you have equipped your system with a PCI controller, changing this allows you to specify which slot has the controller and which PCI interrupt (A, B, C or D) is associated with the connected hard drives.

Remember that this setting refers to the hard disk drive itself, rather than individual partitions. Since each IDE controller supports two separate hard disk drives, you can select the INT# for each. Again, you will note that the primary has a lower interrupt than the secondary as described in " *Slot x Using INT#*" above.

Selecting "*PCI Auto*" allows the system to automatically determine how your IDE disk system is configured.

## Integrated Peripherals

ROM PCI/ISA BIOS (2A59GH2K) INTEGRATED PERIPHERALS AWARD SOFTWARE, INC.		
IDE HDD Block Mode	: Enabled	
IDE Primary Master PIO	: Auto	
IDE Primary Slave PIO	: Auto	
IDE Secondary Master PIO	: Auto	
IDE Secondary Slave PIO	: Auto	
On-Chip Primary PCI IDE	: Enabled	
On-Chip Secondary PCI IDE	: Enabled	
PCI Slot IDE 2nd Channel	: Disabled	
USB Controller	: Disabled	
Onboard FDC Controller	: Enabled	
Onboard Serial Port 1	: Auto	ESC : Quit           ↑↓→← : Select Item F1 : Help           PU/PD/+/- : Modify F5 : Old Values (Shift)F2 : Color F6 : Load BIOS Defaults F7 : Load Setup Defaults
Onboard Serial Port 2	: Auto	
UR2 Mode	: Standard	
Onboard Parallel Port	: 378/IRQ7	
Parallel Port Mode	: SPP	

### IDE HDD Block Mode

This item is used to set IDE HDD Block Mode. If your IDE Hard Disk supports block mode, then you can enable this function to speed up the HDD access time. If not, please disable this function to avoid HDD access error.

### IDE Primary Master/Slave PIO

In these items, there are five modes defined in manual mode and one automatic mode. There are **0**, **1**, **2**, **3**, **4**, and **AUTO** is the default settings for on board Primary Master/Slave PIO timing.

### IDE Secondary Master/Slave PIO

In these items, there are five modes defined in manual mode and one automatic mode. There are **0**, **1**, **2**, **3**, **4**, and **AUTO** is the default settings for on board Secondary Master/Slave PIO timing.

### On-Chip Primary PCI IDE

This item is used to defined on chip Primary PCI IDE controller is "**Enable**" or "**Disable**" setting.

### On-Chip Secondary PCI IDE

This item is used to defined on chip Secondary PCI IDE controller is "**Enable**" or "**Disable**" setting.

### **PCI Slot IDE 2nd channel**

This item is used to defined add-on PCI IDE secondary controller is "*Enable*" or "*Disable*" setting.

### **USB Controller**

This item is used to defined USB controller is " *Enable*" or "*Disable*".

### **Onboard FDC Control**

This item specifies onboard floppy disk drive controller. This setting allows you to connect your floppy disk drives to the onboard floppy connector.

### **Onboard Serial Port 1/Port 2**

These items, Auto or Disabled, is used to define onboard serial port 1/Port2 to *COM1/3F8H*, *COM2/2F8H*, *COM3/3E8H*, *COM4/2E8H*.

### **UR2 Mode**

The system board support IrDA 1.0 and Amplitudes Shift Keyed ASKIR infrared through COM2 port. This item specifies onboard Infra Red mode to *IrDA 1.0*, *ASKIR*, *Standard*, *MIR 1.15M*, *MIR 0.57M*, or *FIR* MIR 1.15, MIR 0.57, and FIR are reserved for future use.

### **UR2 Duplex Mode**

This item specifies onboard infrared transfer mode to *full-duplex* or *half-duplex*.

### **Onboard Parallel Port**

This item specifies onboard parallel port address to *378H*, *278H*, *3BCH* or *Disabled*.

### **Parallel Port Mode**

This item specifies onboard parallel port mode. The options are *SPP* (Standard Parallel Port), *EPP*(Enhanced Parallel Port), *ECP* (Extended Capabilities Port), and *EPP+ECP*.

### **ECP Mode Use DMA**

This item specifies DMA (Direct Memory Access) channel when ECP device is in use. The options are DMA *1* and DMA *3*. This item will not show up when SPP and EPP printer mode is selected

## Password Setting

This section describes the two access modes that can be set using the options found on the Supervisor Password and User Password.

```

ROM PCI/ISA BIOS (2A59GH2B)
CMOS SETUP UTILITY
AWARD SOFTWARE, INC.

STANDARD CMOS SETUP
BIOS FEATURES SETUP
CHIPSET FEATURES SETUP
POWER MANAGEMENT SETUP
PNP/PCI CONFIGURATION
LOAD BIOS DEFAULTS
LOAD SETUP DEFAULTS

INTEGRATED PERIPHERALS
IDE HDD AUTO DETECTION
SUPERVISOR PASSWORD
USER PASSWORD
SAVE & EXIT SETUP

Enter Password: UT SAVING

Esc : Quit
F10 : Save & Exit Setup

↑ ↓ → ← : Select Item
(Shift)F2 : Change Color

Change/Set/Disable Password
  
```

## Supervisor Password and User Password

The options on the Password screen menu make it possible to restrict access to the Setup program by enabling you to set passwords for two different access modes: Supervisor mode and User mode.

In general, Supervisor mode has full access to the Setup options, whereas User mode has restricted access to the options. By setting separate Supervisor and User password, a system supervisor can limit who can change critical Setup values.

## Enter Password

Type the password, up to eight characters, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <Esc> to abort the selection and not enter a password.

To disable password, just press <Enter> when you are prompted to enter password. A message will confirm the password being disabled. Once the password is disabled, the system will boot and you can enter Setup freely.



## **Password Disable**

When you select System at Security Option of BIOS Features Setup Menu, you will be prompted for the password every time the system is rebooted or any time you try to enter Setup. If you select Setup at Security Option of BIOS Features Setup Menu, you will be prompted only when you try to enter Setup.

**Warning :** Retain a record of your password in a safe place. If you forget the password, the only way to access the system is to clear CMOS memory, please refer to "Clear CMOS - JPxx" section .